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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		Attorney Docket No. 01196 U.S. Application No (if known, see 37 CFR 1.5) 09/926489
INTERNATIONAL APPLICATION NO. PCT/FR00/01297	INTERNATIONAL FILING DATE May 12, 2000	PRIORITY DATE CLAIMED May 12, 1999

TITLE OF INVENTION
METHOD AND DEVICE FOR EXTRACTION OF ELECTRODES IN A VACUUM AND EMISSION CATHODES FOR SAID DEVICE

APPLICANT(S) FOR DO/EO/US
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Applicant herewith submits to the United States Designated Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3).
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   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5).

Items 11 to 16 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ As assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:
    Application Data Sheet

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17. ☒ The following fees are submitted: **BASIC NATIONAL FEE (37 CFR 1.492 (a)(1)-(5):** Neither international preliminary examination fee (37 CFR 1.482) Nor international search fee (37 CFR 1.445(a)(2) paid to USPTO And International Search Report not prepared by EPO or JPO..... $1,040.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by EPO or JPO.....$890.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International search fee (37 CFR 1.445(a)(2)) paid to USPTO..... $740.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) But all claims did not satisfy provisions of PCT Article 33(1)-(4).....$710.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) And all claims satisfied provisions of PCT Article 33(1)-(4)..... $100.00	**CALCULATIONS** PTO USE ONLY	
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Total Claims	16 -20=		X $18.00	$	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Group Art Unit:

BINH VU THIEN et al Examiner:

Serial No.: National Phase of PCT/FR00/01297

Filed: concurrently herewith

For: METHOD AND DEVICE FOR EXTRACTION OF ELECTRODES IN A VACUUM AND EMISSION CATHODES FOR SAID DEVICE

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Before calculation of the filing fee, please amend the application as follows:

IN THE CLAIMS:

Please amend the claims as set forth hereinbelow and in the attached appendix:

1. (Amended) A method of extracting in a vacuum (4) electrons emitted from a cathode (2) situated in spaced-apart relationship with an anode (3) which is placed at a given potential relative to the cathode by means of a bias source (5), the method comprising:

· making a cathode (2) presenting at least one junction

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(9) between a metal (7) serving as a reservoir of electrons and an n-type semiconductor (8), the cathode presenting an electron emission surface (11) possessing a surface potential barrier with a height of a few tenths of an electron volt (eV), and presenting thickness lying in the range 1 nm to 20 nm, defined by the value of the lowering desired for the surface potential barrier;

· injecting electrons through the metal/semiconductor junction (9) to create a space charge (Q) in the semiconductor (8) sufficient to lower the surface potential barrier of the semiconductor to a value that is less than or equal to 1 eV relative to the Fermi level of the metal (7); and

· using the bias source (5) that creates an electric field in the vacuum to control the height of the surface potential barrier (V_p) of the n-type semiconductor, so as to modify in reversible manner the electron affinity of the n-type semiconductor surface in order to control the emission of an electron flux towards the anode.

2. (Amended) A method according to claim 1, wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier (V_p) of the n-type semiconductor to be greater than the level of the states occupied by electrons in the n-type semiconductor so as to obtain an emission surface that does

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not emit electrons.

3. (Amended) A method according to claim 1, wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier (V_p) of the n-type semiconductor to be substantially equal to the level of the states occupied by electrons in the n-type semiconductor, in order to obtain an emission surface having low electron affinity.

4. (Amended) A method according to claim 1, wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier of the n-type semiconductor to be lower than the level of the states occupied by electrons in the n-type semiconductor so as to obtain an emission surface of negative electron affinity.

5. (Amended) A method according to claim 1 wherein the temperature of the cathode (2) is controlled in order to control the flux of the emitted electron beam.

8. (Amended) An electron emission cathode for a device for extracting an electron beam in a vacuum in accordance with claim 6, the cathode being characterized in that it comprises:

· a first portion forming an electron reservoir and constituted by at least one metal layer (7); and

· a second portion forming a conduction medium for the

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electrons injected into the metal layer and formed by an n-type semiconductor (8) co-operating with the metal layer to define a metal/semiconductor junction (9) possessing a potential barrier with a height of a few tenths of an electron volt, the n-type semiconductor presenting an emission surface (11) for the electrons, and possessing thickness lying in the range 1 nm to 20 nm defined by the value of the lowering desired for the surface potential barrier.

Please cancel claims 17 and 18 without prejudice or disclaimer of the subject matter thereof.

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REMARKS

The claims have been amended to delete all multiple dependencies and to otherwise place the claims in better form for US practice.

Respectfully submitted,

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APPENDIX

IN THE CLAIMS:

1. (Amended) A method of extracting in a vacuum (4) electrons emitted from a cathode (2) situated in spaced-apart relationship with an anode (3) which is placed at a given potential relative to the cathode by means of a bias source (5), the method [being characterized in that it consists in] comprising:

· making a cathode (2) presenting at least one junction (9) between a metal (7) serving as a reservoir of electrons and an n-type semiconductor (8), the cathode presenting an electron emission surface (11) possessing a surface potential barrier with a height of a few tenths of an electron volt (eV), and presenting thickness lying in the range 1 nm to 20 nm, defined by the value of the lowering desired for the surface potential barrier;

· injecting electrons through the metal/semiconductor junction (9) to create a space charge (Q) in the semiconductor (8) sufficient to lower the surface potential barrier of the semiconductor to a value that is less than or equal to 1 eV relative to the Fermi level of the metal (7); and

· using the bias source (5) that creates an electric field in the vacuum to control the height of the surface potential barrier (V_p) of the n-type semiconductor, so as to modify in

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reversible manner the electron affinity of the n-type semiconductor surface in order to control the emission of an electron flux towards the anode.

2. (Amended) A method according to claim 1, [characterized in that it consists in controlling] wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier (V_p) of the n-type semiconductor to be greater than the level of the states occupied by electrons in the n-type semiconductor so as to obtain an emission surface that does not emit electrons.

3. (Amended) A method according to claim 1, [characterized in that it consists in controlling] wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier (V_p) of the n-type semiconductor to be substantially equal to the level of the states occupied by electrons in the n-type semiconductor, in order to obtain an emission surface having low electron affinity.

4. (Amended) A method according to claim 1, [characterized in that it consists in controlling] wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier of the n-type semiconductor to be lower than the level

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of the states occupied by electrons in the n-type semiconductor so as to obtain an emission surface of negative electron affinity.

5. (Amended) A method according to [any one of claims] claim 1[, 3, or 4, characterized in that it consists in controlling] wherein the temperature of the cathode (2) is controlled in order to control the flux of the emitted electron beam.

8. (Amended) An electron emission cathode for a device for extracting an electron beam in a vacuum in accordance with claim 6 [or claim 7], the cathode being characterized in that it comprises:

· a first portion forming an electron reservoir and constituted by at least one metal layer (7); and

· a second portion forming a conduction medium for the electrons injected into the metal layer and formed by an n-type semiconductor (8) co-operating with the metal layer to define a metal/semiconductor junction (9) possessing a potential barrier with a height of a few tenths of an electron volt, the n-type semiconductor presenting an emission surface (11) for the electrons, and possessing thickness lying in the range 1 nm to 20 nm defined by the value of the lowering desired for the surface potential barrier.

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8/PRTS

A METHOD AND A DEVICE FOR EXTRACTING ELECTRONS IN A VACUUM, AND EMISSION CATHODES FOR SUCH A DEVICE

TECHNICAL FIELD

The present invention relates to the field of emitting electrons in a vacuum from a cathode in the broad sense.

The subject matter of the invention thus covers the field of electron sources in the broad sense suitable for use in electronic devices or for making flat screens, in particular.

PRIOR ART

In conventional manner, an electron extractor device comprises an emission cathode and an anode spaced apart from each other with a vacuum or an ultrahigh vacuum existing between them. The anode and the cathode are interconnected by means of a bias source serving to place them at a given relative potential.

In order to ensure that a constant flow of electrons is emitted into the vacuum from the cathode, it is necessary to extract the electrons from the potential in which they are trapped in the cathode material. Electrons can be extracted from the cathode by the technique of heating the cathode, so as to raise the energy of the electrons to a value which exceeds the work of emission which depends on the surface state of the cathode. That technique is known as thermionic emission and suffers from the drawback of requiring the cathode to be at high temperature (2700 kelvins (K) for a tungsten cathode, for example) and consequently of consuming relatively large amounts of energy and dissipating it as heat. Furthermore, that thermionic technique of emitting electrons does not enable localized electron emission sites to be obtained.

A second technique for extracting electrons is known in which the surface potential barrier of the cathode is

deformed by means of an intense electric field. The height of the potential barrier depends only on the surface state of the cathode. That technique is known as field emission and it enables electrons to be emitted at a so-called "cold" temperature (300 K or less). A drawback of that technique lies in the need to implement a high vacuum (10^{-10} Torr) in order to stabilize the electron emission current. Furthermore, in order to obtain an intense electric field, the cathode must necessarily be shaped so present a sharp point, and practical implementation of an array of points raises problems that are quite difficult. Furthermore, that technique does not enable electrons to be emitted in uniform manner from a plane surface.

Document WO 98/06135 discloses a device for extracting electrons which comprises a cathode situated at a distance from an anode. The cathode is constituted by a semiconductive film defining an emission surface for electrons and supported by an injection electrode. The emission surface has a front electrode enabling the injection electrode to be biased, so as to define the potential at the surface of the semiconductive film. Controlling this bias voltage enables electrons to be extracted from the cathode and enables the emission of electron flux towards the anode to be controlled.

It should be observed that electron emission is due to a thermionic phenomenon insofar as the electrons are excited by the energy contribution coming from electrons injected by the injection electrodes. Furthermore, the shape of the cathode requires technical means to be implemented that are difficult to achieve in practice.

An analysis of previously known techniques leads to the observation that there is a need for a technique that enables electrons to be extracted at low temperature and low electric field in a soft vacuum (as from 10^{-4} Torr), from an emission surface that is localized or uniform and

that does not present particular problems of practical implementation.

SUMMARY OF THE INVENTION

The invention seeks to satisfy this need by proposing a method enabling the various objects specified above to be satisfied.

Accordingly, the invention provides a method of extracting electrons in a vacuum that are emitted from a cathode situated at a distance from an anode which is placed at a given potential relative to the cathode, by means of a bias source. According to the invention, the method consists in:

· making a cathode presenting at least one junction between a metal serving as a reservoir of electrons and an n-type semiconductor, the cathode presenting an electron emission surface possessing a surface potential barrier with a height of a few tenths of an electron volt (eV), and presenting thickness lying in the range 1 nanometer (nm) to 20 nm, defined by the value of the lowering desired for the surface potential barrier;

· injecting electrons through the metal/semiconductor junction to create a space charge in the semiconductor sufficient to lower the surface potential barrier of the semiconductor to a value that is less than or equal to 1 eV relative to the Fermi level of the metal; and

· using the bias source that creates an electric field in the vacuum to control the height of the surface potential barrier of the n-type semiconductor, so as to modify in reversible manner the electron affinity of the n-type semiconductor surface in order to control the emission of an electron flux towards the anode.

The invention also provides a device for extracting electrons in a vacuum as emitted from a cathode situated at a distance from at least one anode placed at a given potential relative to the cathode by means of a bias

source. According to the invention, the device comprises:

· an emission cathode having at least one junction between a metal and an n-type semiconductor, possessing a surface potential barrier with a height of a few tenths of an electron volt, the n-type semiconductor presenting an emission surface for electrons and possessing thickness lying in the range 1 nm to 20 nm defined by the value of the lowering desired for the surface potential barrier; and

· a bias source creating an electric field in the vacuum serving firstly to inject electrons through the metal/semiconductor junction so as to create a space charge in the semiconductor sufficient to lower the surface potential barrier of the semiconductor to a value that is less than or equal to 1 eV relative to the Fermi level of the metal, and also to control the height of the surface potential barrier of the n-type semiconductor, i.e. to reversibly modify the electron affinity of the surface of the n-type semiconductor in order to control electron flux emission.

The invention also provides a novel electron-emission cathode for a cathode extraction device, the cathode comprising:

· a first portion forming an electron reservoir and constituted by at least one metal layer; and

· a second portion forming a conduction medium for the electrons injected into the metal layer and formed by an n-type semiconductor co-operating with the metal layer to define a metal/semiconductor junction possessing a potential barrier with a height of a few tenths of an electron volt, the n-type semiconductor presenting an emission surface for the electrons, and possessing thickness lying in the range 1 nm to 20 nm defined by the value of the lowering desired for the surface potential barrier.

Various other characteristics appear from the following description made with reference to the accompanying drawings which show embodiments and implementations of the invention as non-limiting examples.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram showing a device for extracting electrons in a vacuum in accordance with the invention.

Figure 2 is an energy-band diagram when the metal is initially separate from the semiconductor, for explaining the principle of the invention.

Figure 2bis is a diagram showing the energy bands E (eV) for the cathode as a function of the position x taken in the cathode-anode direction.

Figures 3, 4, and 5 are energy-band diagrams at the cathode as obtained during three characteristic stages of the method of the invention.

Figure 6 is a graph showing how the current obtained varies as a function of the applied bias voltage.

Figure 7 is a diagram showing how the resulting emission current varies as a function of time for different bias voltage values.

Figures 8, 9, and 10 show various embodiments of a plane cathode enabling the method of the invention to be implemented.

BEST METHOD OF PERFORMING THE INVENTION

As can be seen in Figure 1, the subject matter of the invention relates to a device 1 enabling electrons to be extracted in a vacuum, the device comprising an emission cathode 2 spaced apart from at least one anode 3 which in the example shown constitutes an anode for receiving electrons emitted by the cathode 2. The cathode 2 and the anode 3 define between them a volume 4 in which there is a vacuum (10^{-4} Torr to 10^{-8} Torr) or an

ultrahigh vacuum (10^{-8} Torr to 10^{-12} Torr). The extraction device 1 also comprises a bias source 5 enabling the cathode 2 to be placed at a given potential relative to the anode 3. Practical implementation of the extraction device 1 is not described in greater detail below insofar as it is well known in the state of the art.

In accordance with the invention, the extraction device 1 comprises an emission cathode 2 having a first portion 7 forming an electron reservoir and constituted by at least one metal layer. The emission cathode 2 also has a second portion 8 forming a conduction medium for injected electrons. The conduction medium 8 is formed by an n-type semiconductor co-operating with the metal layer 7 to define a metal/semiconductor (Schottky) electron junction 9. According to an advantageous characteristic of the invention, the Schottky junction 9 has a potential barrier to a height of a few tenths of an electron volt, i.e. lying in the range 0.05 eV to 1 eV, and preferably about 0.1 eV. The characteristics of this Schottky junction require an appropriate pair of metal 7 and n-type semiconductor 8 to be selected. For example, when the metal 7 is platinum, the semiconductor layer 8 can be either n-type silicon carbide (SiC) or n-type rutile (TiO_2) obtained by sputtering.

According to another advantageous characteristic of the invention, the n-type semiconductor presents an emission surface 11 for electrons extracted in a vacuum 4. The semiconductor 8 presents defined thickness between the Schottky junction 9 and the emission surface 11, said thickness lying in the range 1 nm to 20 nm. The value of this thickness is defined by the amount of lowering desired for the surface potential barrier. By way of example, the thickness of the semiconductor 8 can be about 5 nm for semiconductor layers of n-type silicon carbide (SiC) or of n-type rutile or titanium dioxide (TiO_2) on a metal layer of platinum. In a preferred embodiment, the semiconductor 8 is a large-gap n-type

semiconductor, i.e. it has a gap greater than or equal to 3 eV.

Figure 2 shows the energy bands of the metal layer 7 and of the semiconductor 8 relative to the vacuum 4 when they are separate from one another. The metal layer 7 has a Fermi level E_f and work of emission Φ_m between the Fermi level and the potential level V_0 of the vacuum 4. The semiconductor 8 presents a forbidden band of width E_g, a conduction band of level E_c, a Fermi level E_f, and electron affinity χ relative to the potential level V_0 of the vacuum 4. While the Schottky junction is being made between the metal layer 7 and the n-type semiconductor 8, energy adjustment occurs leading to the same Fermi level and potential of the vacuum 4. Thus, as can be seen in Figure 2bis, the cathode 2 as made in this way presents a metal layer 7 with a Fermi level E_f and co-operating with the n-type semiconductor 8 to define a Schottky junction 9. At the surface 11 of the semiconductor 8, there exists a surface potential barrier V_p.

The extraction device 1 of the invention uses the bias source 5 to enable electrons to be emitted by means of a two-stage serial process. The first stage represents injecting electrons into the semiconductor 8 to form a space charge Q that is sufficient to lower the surface potential barrier V_p of the semiconductor 8 to a value which is less than or equal to 1 eV relative to the Fermi level of the metal 7. This first stage is followed by a second stage which consists in reversibly regulating the emission of electrons towards the anode 3 by means of the bias source 5 creating an electric field F in the vacuum 4 that enables the height of the surface potential barrier V_p of the semiconductor 8 to be controlled.

Figure 2bis illustrates the process whereby electrons are emitted by two consecutive stages. In the first stage et_1, the surface potential barrier V_p of the semiconductor 8 is lowered to a value which is less than or equal to 1 eV relative to the Fermi level E_f of the

metal 7. The energy difference between the maximum value of the surface potential barrier on the semiconductor 8 and the Fermi level of the metal 7 is represented by $\Delta\Phi E$. This lowering of the surface potential barrier of the semiconductor 8 (passing from curve C_0 to curve C_1) is due to electrons being injected under the influence of the bias source 5 through the junction 9 and to space charge Q being created in the semiconductor 8. The lowering of the surface potential barrier of the semiconductor 8 is an increasing function of the space charge Q which is itself an inverse function of the thickness of the semiconductor 8.

During the second stage et_2, electrons are emitted towards the anode 3 under the control of the bias source 5 which establishes a variable electric field F in the vacuum 4 thus enabling the surface potential barrier V_p to be modulated. The surface potential barrier V_p (curves C_1, C_2, C_3) is lowered for increasingly high values of the electric field F. The stage et_2 can thus be observed to comprise three characteristic behaviors for the cathode relative to the value of the electric field F created in the vacuum by the bias source 5, as shown more particularly in Figures 3 to 5.

Figure 3 shows a first behavior of the anode 2 in which the voltage applied by the bias source 5 is lower than a threshold value V_s from which an electron current can be measured. At this voltage value, an electric field F is applied which leads to a first lowering a_1 of the height of the surface potential barrier that results from the band being curved due to penetration of the electric field F and to a space charge Q being created by electrons being injected from the metal 7 into the semiconductor 8. A lowering a_2 is also obtained of the height of the surface potential barrier of the semiconductor because of the Schottky effect. It should be observed that the presence of the electric field F also leads to the surface potential barrier of the semiconductor 8

being deformed. In the example shown in Figure 3, the total lowering of the potential (a_1+a_2) of the surface potential barrier V_p of the semiconductor, as obtained by a given electric field corresponding to a voltage that is low and less than the threshold value V_s is not sufficient to allow electrons to be emitted. The surface potential barrier V_p is thus too high to enable electrons to be emitted into the vacuum 4. The electrons injected through the electron junction 9 are trapped inside the semiconductor 8. It must be assumed that the height of the surface potential barrier of the n-type semiconductor is greater than the level of the states occupied by the electrons in the semiconductor 8. Portion A of Figure 6 shows the curve of current I as a function of the potential V of the source 5, giving the current characteristic as obtained during this first stage of operation.

Figure 4 shows a second characteristic behavior of the anode 2 for an applied bias voltage that is greater than the threshold voltage V_s. The electric field F created in this way is such that the height of the surface potential barrier V_p of the semiconductor 8 is substantially equal to the level of the states occupied by electrons in the semiconductor. The lowering (a_1+a_2) of the height of the surface potential barrier V_p of the semiconductor is then sufficient to enable electrons to escape by the tunnel effect. This produces an emission surface 11 having low electron affinity resulting from the presence of the space charge Q and the penetration of the electric field. The field emission current I shown in portion B of the curve of Figure 6 is governed by the Fowler Nordheim relationship characteristic of electron emission by the tunnel effect.

Figure 5 shows a third characteristic behavior of the cathode when the bias voltage V is much greater than the threshold voltage V_s. The bias voltage V is such that the electric field F created is adapted so that the

height of the surface potential barrier V_p of the semiconductor 8 is lower than the level of the states occupied by the electrons in the semiconductor 8. Surface emission 11 is thus obtained with negative electron affinity. The mechanism whereby the electrons are emitted is a kind of thermionic emission considering that electron injection is obtained from the metal/semiconductor junction 9. Portion C of the curve in Figure 6 shows the form of the current I as a function of the applied voltage V for this third behavior. It must be understood that current emission operating under thermionic conditions is insensitive to small variations in the vacuum barrier due to adsorption. As can be seen more clearly in Figure 7, current stability increases with increasing bias voltage V because electron injection is unaffected by the modifications that can appear in the vacuum 4.

The method of the invention thus makes it possible to control the emission of a flux of electrons by controlling the height of the surface potential barrier V_p of the semiconductor 8 which is directly associated with the value of the bias voltage V. In this second stage, surface emission can be obtained that does not emit electrons (Figure 3), that presents low electron affinity (Figure 4), or negative electron affinity (Figure 5).

A technical advantage of the invention is to present an injection interface which is a solid junction between a metal and a semiconductor. Electron injection is thus protected from influences of the environment, such as the phenomena of adsorption, desorption, ion bombardment, etc. In addition, the emission surface of the cathode after the first stage et_1 is a surface having low or negative electron affinity. Electron emission is practically insensitive to influences from the environment, such as the phenomena of adsorption, desorption, ion bombardment, etc. Furthermore, it should be observed that the emission current is very sensitive

to temperature, so provision can be made to control the temperature of the cathode in order to control the flux of the emitted electron beam.

From the above, it can be seen that the emission surface depends directly on the electric field distribution on the emission surface 11 of the cathode. Thus, the presence of protuberances or projections on the emission face 11 can serve to confine electron emission to such projections. Naturally, it can also be envisaged to cause electrons to be emitted from a surface that is plane.

Figures 8 to 10 show various embodiments of a cathode 2 for implementing the extraction method of the invention. According to an advantage of the invention, the cathode 2 can be made using planar fabrication technologies that are conventional in microelectronics.

Figure 8 shows a cathode 2 comprising a first portion forming an electron reservoir and constituted by a metal layer 7 carried by a substrate 13 that is metallic, semiconductive, or insulating. The metal layer 7 is coated in an n-type semiconductor layer 8 enabling the Schottky junction 9 to be implemented. The semiconductor layer 8 is made using conventional microelectronic doping technologies, such as ion implanting or deposition, e.g. of the chemical vapor deposition (CVD) type, sputtering, evaporation, in a vacuum, or physical vapor deposition (PVD). In this embodiment, the emission surface 11 is substantially plane. In another embodiment that can be seen in Figure 9, an emission surface 11 is made that presents protuberances or projections 14 at determined locations. For this purpose, a substrate 13 is made out of a semiconductor or a metal whose place for receiving the metal layer 7 is etched by lithographic techniques so as to make projections that are to receive superposed thereon the metal layer 7 and the n-type semiconductor layer 8. As can be seen clearly in Figure 9, the semiconductor

element 8 thus presents an emission surface 11 with localized zones 14 for space confinement of emission electrons at the tips of the projections 14.

Figure 10 shows another variant embodiment of a cathode of the invention comprising a metal layer 7 deposited on an insulating substrate 13. The assembly made in this way is subjected to ion bombardment so as to enable point-shaped projections 15 to appear that also form n-type semiconductor elements 8. A metal/semiconductor junction 9 thus appears where the projection passes through the metal layer 7.

There are numerous applications for the electron extraction device of the invention in the field of electronics, in particular for constituting a source for vacuum electronic components or for making flat screens. In the application of the invention for making flat screens, provision can be made in conventional manner to implement a first electron extraction electrode which is placed close to the anode and allowing electron beams to pass of an intensity that is modulated locally for each pixel of the screen. These beams are picked up by a reception anode placed downstream from the extraction anode relative to the emission cathode. It should be observed that by making the substrate 13 carrying the metal layer 7 out of a semiconductor material, it is possible to integrate active electronic components in the substrate for the purpose of locally controlling the emission of electrons.

Another particularly advantageous application of the subject matter of the invention lies in producing parallel and uniform electron beams for projection electron lithography.

In the embodiments described with reference to Figures 8 to 10, the substrate 13 is plane in shape. This shape is particularly suitable for devices that require a planar electron source (e.g. flat screens that can reach dimensions of square meter (m^2) order or more,

electronic components of smaller dimensions, of square millimeter (mm^2) order, or of the order of several tens of square centimeters (cm^2)). Naturally, the substrate 13 can have other types of shape as a function of the application. For example, the substrate 13 can be in the form of an individual point or an individual pinhead for making cathodes in individual electron guns. Such guns are used in particular in electron microscopes and in cathode ray tubes (CRTs).

The invention is not limited to the examples described and shown since numerous modifications can be applied thereto without going beyond the ambit of the invention.

CLAIMS

1/ A method of extracting in a vacuum (4) electrons emitted from a cathode (2) situated in spaced-apart relationship with an anode (3) which is placed at a given potential relative to the cathode by means of a bias source (5), the method being characterized in that it consists in:

· making a cathode (2) presenting at least one junction (9) between a metal (7) serving as a reservoir of electrons and an n-type semiconductor (8), the cathode presenting an electron emission surface (11) possessing a surface potential barrier with a height of a few tenths of an electron volt (eV), and presenting thickness lying in the range 1 nm to 20 nm, defined by the value of the lowering desired for the surface potential barrier;

· injecting electrons through the metal/semiconductor junction (9) to create a space charge (Q) in the semiconductor (8) sufficient to lower the surface potential barrier of the semiconductor to a value that is less than or equal to 1 eV relative to the Fermi level of the metal (7); and

· using the bias source (5) that creates an electric field in the vacuum to control the height of the surface potential barrier (V_p) of the n-type semiconductor, so as to modify in reversible manner the electron affinity of the n-type semiconductor surface in order to control the emission of an electron flux towards the anode.

2/ A method according to claim 1, characterized in that it consists in controlling the bias source (5) so as to create an electric field suitable for causing the height of the surface potential barrier (V_p) of the n-type semiconductor to be greater than the level of the states occupied by electrons in the n-type semiconductor so as to obtain an emission surface that does not emit electrons.

3/ A method according to claim 1, characterized in that it consists in controlling the bias source (5) so as to create an electric field suitable for causing the height of the surface potential barrier (V_p) of the n-type semiconductor to be substantially equal to the level of the states occupied by electrons in the n-type semiconductor, in order to obtain an emission surface having low electron affinity.

4/ A method according to claim 1, characterized in that it consists in controlling the bias source (5) so as to create an electric field suitable for causing the height of the surface potential barrier of the n-type semiconductor to be lower than the level of the states occupied by electrons in the n-type semiconductor so as to obtain an emission surface of negative electron affinity.

5/ A method according to any one of claims 1, 3, or 4, characterized in that it consists in controlling the temperature of the cathode (2) in order to control the flux of the emitted electron beam.

6/ A device for extracting in a vacuum (4) electrons emitted from a cathode (2) situated in a spaced-apart relationship with at least one anode (3) placed at a given potential relative to the cathode by means of a bias source (5), the device being characterized in that it comprises:

· an emission cathode (2) having at least one junction (9) between a metal (7) and an n-type semiconductor (8), possessing a surface potential barrier with a height of a few tenths of an electron volt, the n-type semiconductor presenting an emission surface for electrons and possessing thickness lying in the range 1 nm to 20 nm defined by the value of the lowering desired for the surface potential barrier; and

· a bias source (5) creating an electric field in the vacuum (4) serving firstly to inject electrons through the metal/semiconductor junction (9) so as to create a space charge (Q) in the semiconductor (8) sufficient to lower the surface potential barrier of the semiconductor to a value that is less than or equal to 1 eV relative to the Fermi level of the metal (7), and also to control the height of the surface potential barrier of the n-type semiconductor, i.e. to reversibly modify the electron affinity of the surface of the n-type semiconductor in order to control electron flux emission.

7/ A device according to claim 6, characterized in that it includes an electron extraction electrode followed by an anode for receiving the extracted electrons.

8/ An electron emission cathode for a device for extracting an electron beam in a vacuum in accordance with claim 6 or claim 7, the cathode being characterized in that it comprises:

· a first portion forming an electron reservoir and constituted by at least one metal layer (7); and

· a second portion forming a conduction medium for the electrons injected into the metal layer and formed by an n-type semiconductor (8) co-operating with the metal layer to define a metal/semiconductor junction (9) possessing a potential barrier with a height of a few tenths of an electron volt, the n-type semiconductor presenting an emission surface (11) for the electrons, and possessing thickness lying in the range 1 nm to 20 nm defined by the value of the lowering desired for the surface potential barrier.

9/ An emission cathode according to claim 8, characterized in that the electron junction possesses a potential barrier of height lying in the range 0.05 eV to 0.5 eV, and preferably approximately 0.1 eV.

10/ A cathode according to claim 8, characterized in that the first portion forming an electron reservoir is formed by a metal layer (7) carried on a substrate (13) of metal, semiconductor, or insulation.

11/ A cathode according to claim 8, characterized in that the n-type semiconductor (8) possesses an emission surface (11) for electrons that is substantially plane.

12/ A cathode according to claim 8, characterized in that the n-type semiconductor (8) possesses an emission surface (11) for electrons that presents projections (14, 15) enabling electron emission to be confined in register with each of them.

13/ A cathode according to claim 11, characterized in that the n-type semiconductor (8) possesses an emission surface (11) for electrons presenting projections (14) made in determined locations by lithographic techniques.

14/ A cathode according to claim 11, characterized in that the n-type semiconductor (8) possesses an emission surface for electrons presenting projections (15) in the form of points, obtained by ion bombardment of the metal layer deposited on an insulating substrate.

15/ A cathode according to claim 8, characterized in that the first portion forming an electron reservoir is constituted by a metal layer (7) carried by a semi-conductor substrate having active components arranged therein for locally controlling electron emission.

16/ A cathode according to claim 10, characterized in that the substrate (13) possesses an individual point shape or an individual pinhead shape for use in an individual electron gun.

17/ The use of a cathode according to any one of claims 10 to 15, for producing parallel and uniform electron beams for projection electron lithography.

18/ The use of a cathode according to any one of claims 10 to 15, for producing parallel electron beams of intensity that is modulated locally for each pixel of a flat screen.

A B S T R A C T

A METHOD AND A DEVICE FOR EXTRACTING ELECTRONS IN A VACUUM, AND EMISSION CATHODES FOR SUCH A DEVICE

The method of the invention for extracting electrons in a vacuum consists in:

· making a cathode presenting at least one junction (9) between a metal (7) acting as an electron reservoir and an n-type semiconductor (8) possessing a surface potential barrier with a height of a few tenths of an electron volt, and presenting thickness lying in the range 1 nm to 20 nm;

· injecting electrons through the metal/semiconductor junction (9) to create a space charge in the semiconductor (8) sufficient to lower the surface potential barrier of the semiconductor to a value that is less than or equal to 1 eV relative to the Fermi level of the metal (7); and

· using the bias source creating an electric field in the vacuum to control the height of the surface potential barrier (V_p) of the n-type semiconductor in order to control the emission of the electron flux towards the anode.

Translation of the title and the abstract as they were when originally filed by the Applicant. No account has been taken of any changes that may have been made subsequently by the PCT Authorities acting ex officio, e.g. under PCT Rules 37.2, 38.2, and/or 48.3.

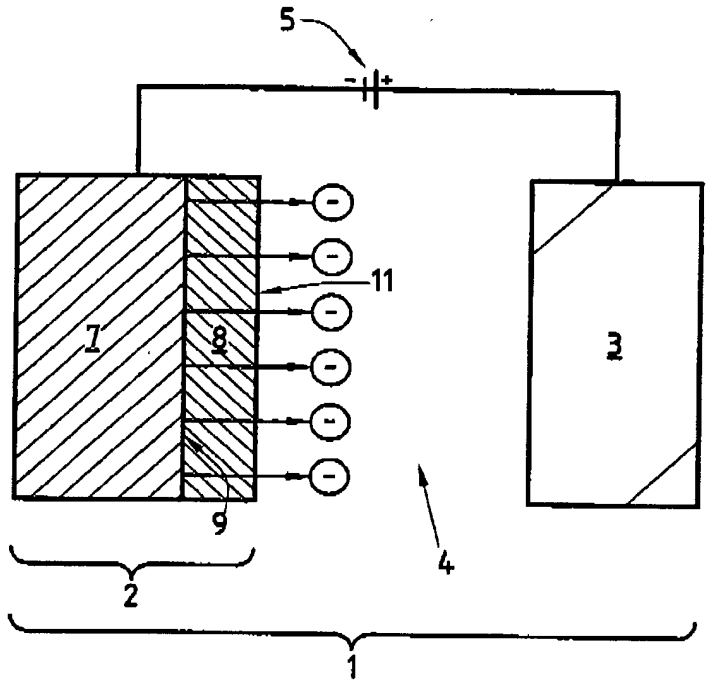
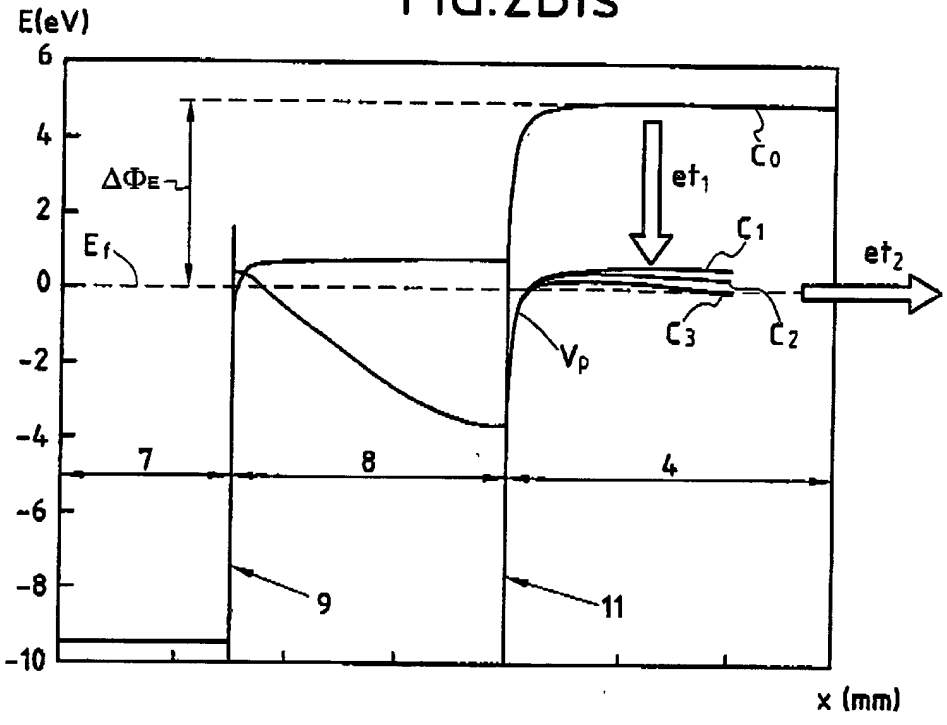


FIG.1

FIG.2Bis



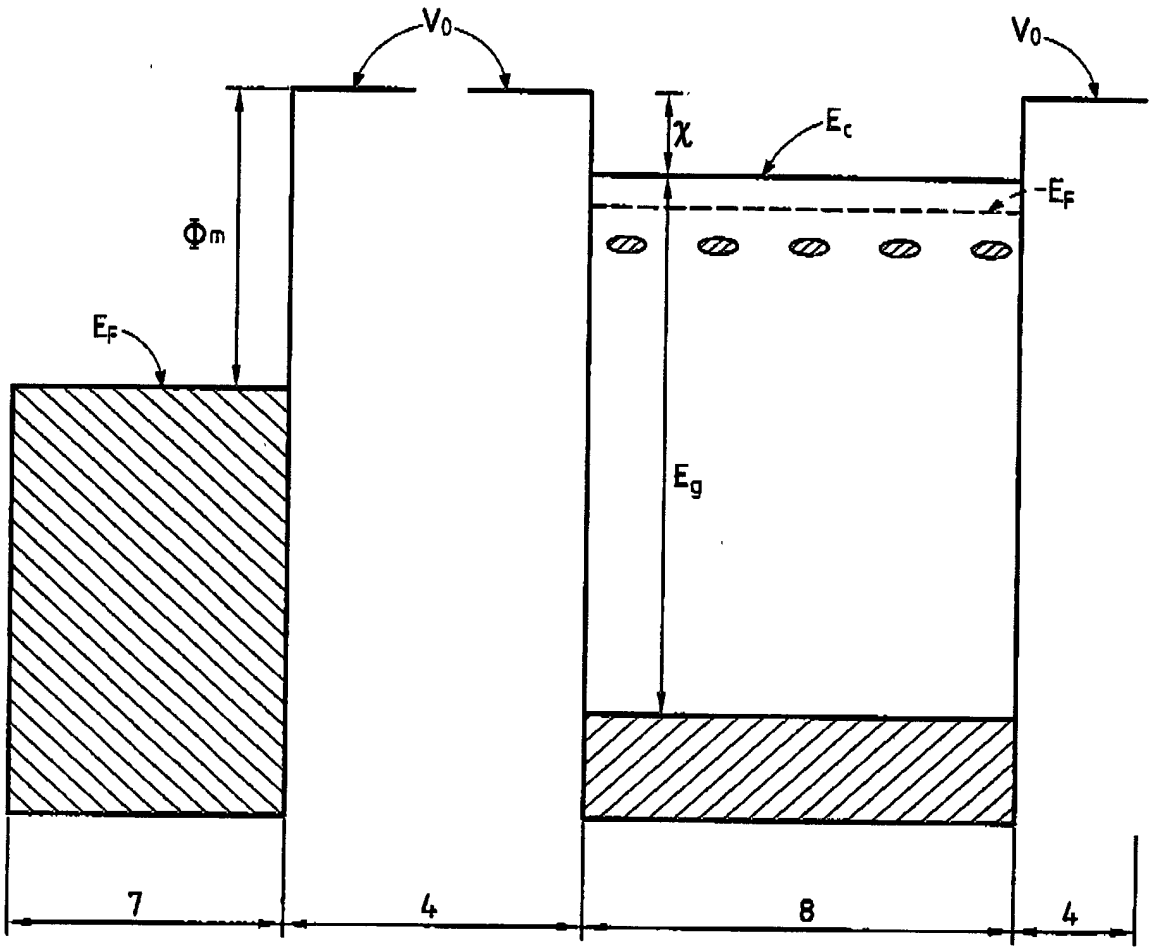


FIG.2

09/926489

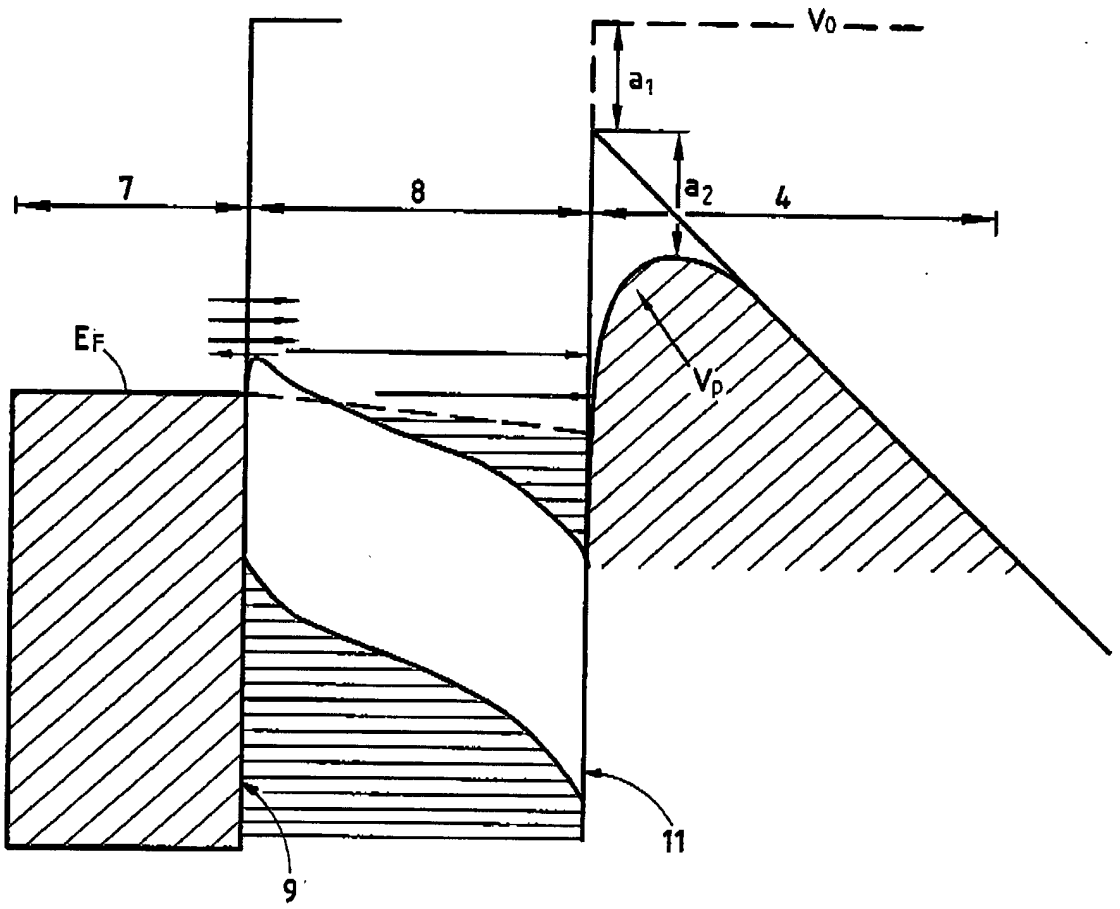


FIG.3

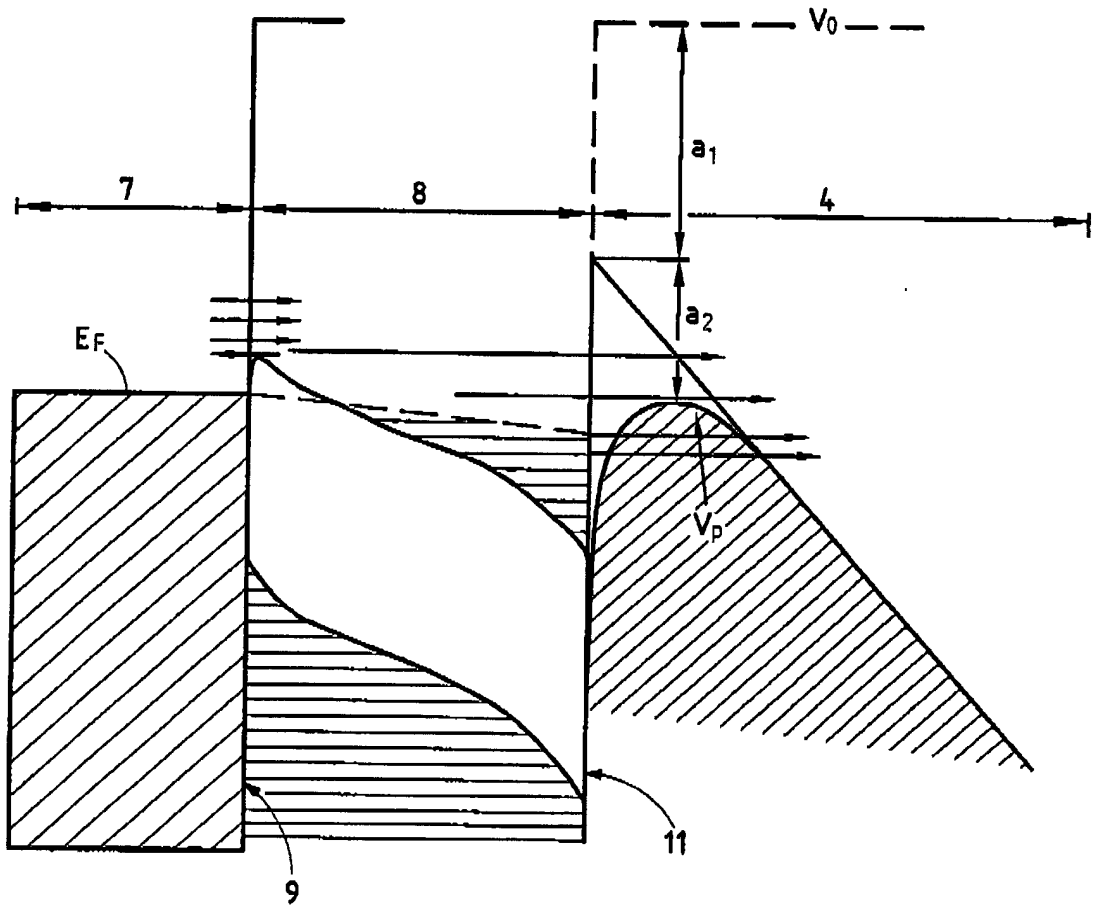


FIG.4

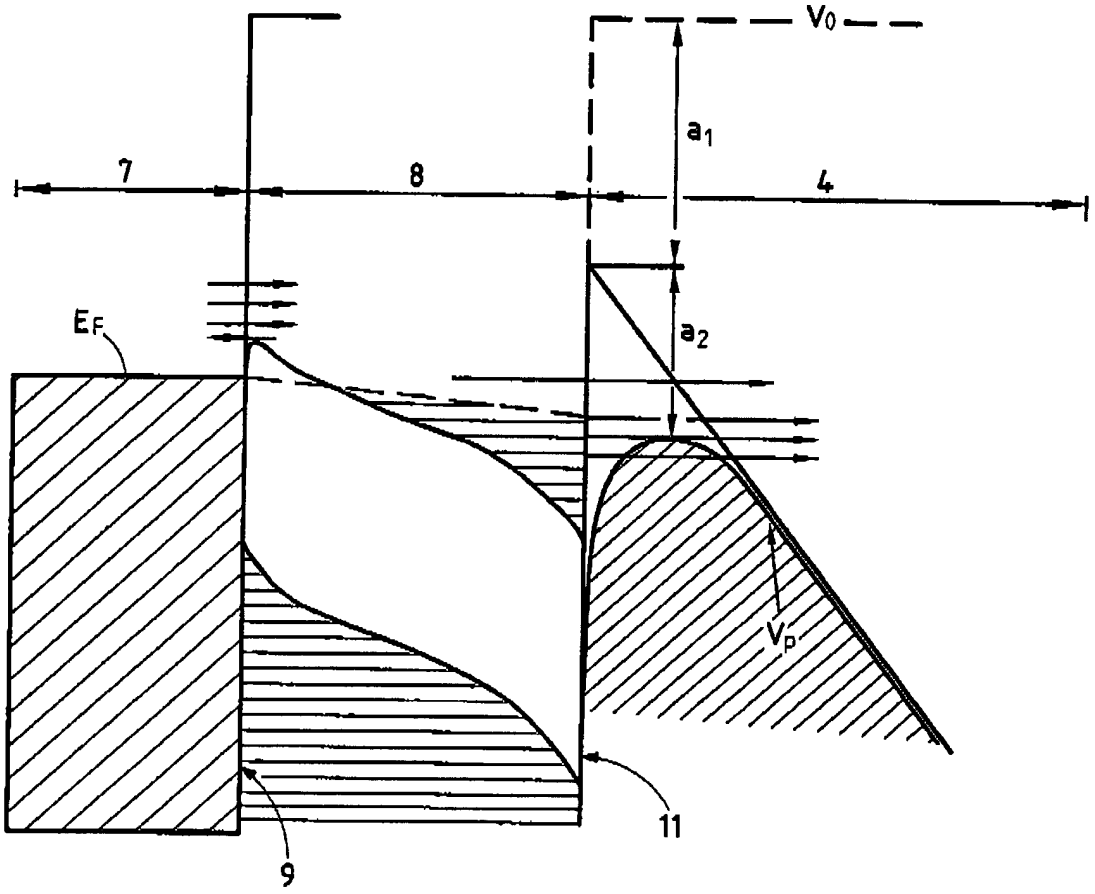


FIG.5

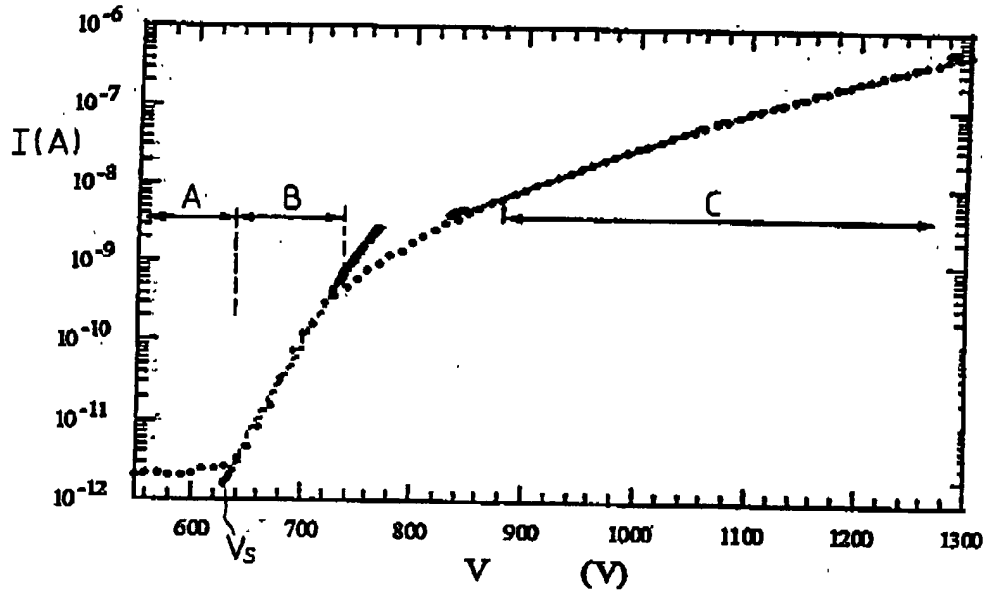

I(A)
10-6
10-7
10-8
10-9
10-10
10-11
10-12
A
B
C
600
700
800
900
1000
1100
1200
1300
Vs
V (V)

FIG.6

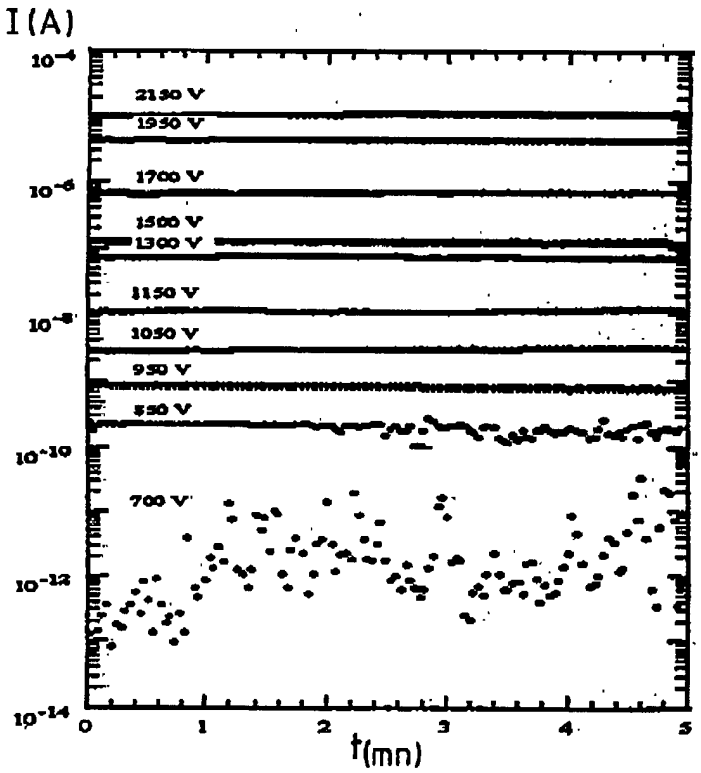

I(A)
10⁻⁴
10⁻⁶
10⁻⁸
10⁻¹⁰
10⁻¹²
10⁻¹⁴
2130 V
1950 V
1700 V
1500 V
1300 V
1150 V
1050 V
950 V
850 V
700 V
0
1
2
3
4
5
t(mn)

FIG.7

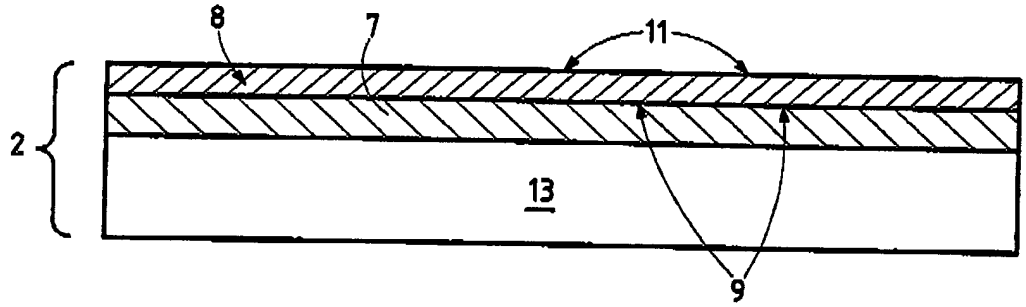


FIG.8

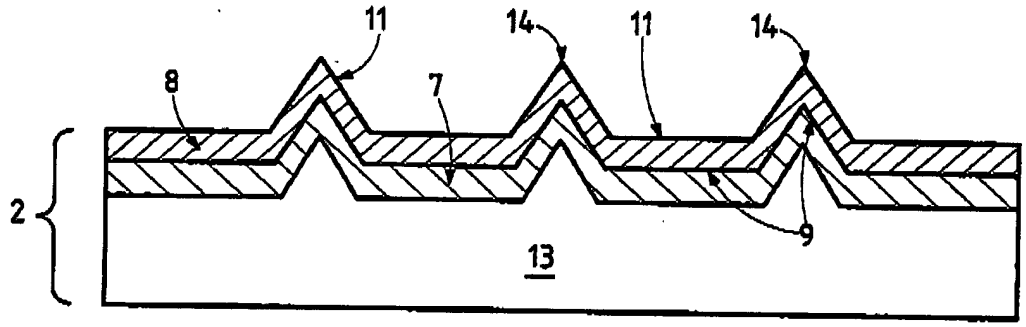


FIG.9

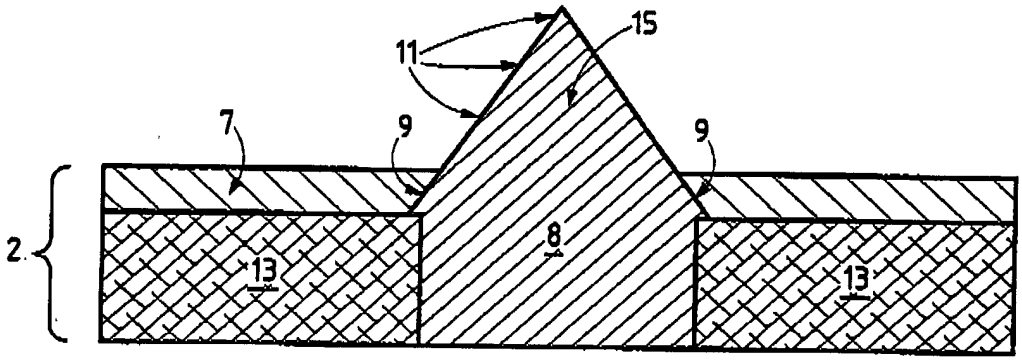


FIG.10

DECLARATION FOR PATENT APPLICATION

Docket No. 09/926489

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Method and device for extraction of electrodes in a vacuum and emission cathodes for said device

the specification of which

(check one) is described and claimed in PCT International Application .PCT/FR00/01 297 filed on MAY 12, 2000 amended on APRIL 26, 2001 (if applicable) (OR) is described in United States Application Number filed on (MM/DD/YYYY) (OR) is attached hereto

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).
I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
(Number)	(Country)	(Day/Month/Year Filed)	Yes No
99 06 254	FRANCE	MAY 12, 1999	X

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (Filing Date) (Status-patented, pending, a7a-nTo-n-eR1)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Donald L. Dennison Reg. No. 19920
William H. Meserole Reg. No. 20833
Burton Scheiner Reg. No. 24018
Ira J. Schultz Reg. No. 28666
Scott T. Wakeman Reg. No. 37750

SEND CORRESPONDENCE TO:
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1745 Jefferson Davis Highway, Suite 612
Arlington, Virginia 22A

DIRECT TELEPHONE CALLS TO:
(name and telephone number)
(703) 412-1155 Ext.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor. **VU THIEN Binh**

Inventor's signature Vu Thien Binh Date 27 Nov. 2001
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Inventor's signature Date 27 Nov. 2001
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Post Office Address 8 rue Jules Kumer - 69100 VILLEURBANNE (FRANCE)

Full name of third joint inventor **THEVENARD Paul**

Inventor's signature Date 27 Nov. 2001
Residence 9 rue Guyot - 69300 CALUIRE (FRANCE) Citizenship FRANCE
Post Office Address 9 rue Guyot - 69300 CALUIRE (FRANCE)

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

Attorney Docket No. 01196

U.S. Application No (if known, see 37 CFR 1.5) 09/926489

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR00/01297	May 12, 2000	May 12, 1999

TITLE OF INVENTION
METHOD AND DEVICE FOR EXTRACTION OF ELECTRODES IN A VACUUM AND EMISSION CATHODES FOR SAID DEVICE

APPLICANT(S) FOR DO/EO/US
Binh Vu Thien, Jean-Pierre Dupin and Paul Thevenard

Applicant herewith submits to the United States Designated Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3).
   a. ☐ are transmitted herewith (only if not required by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5).

Items 11 to 16 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ As assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:
    Application Data Sheet

17. ☒ The following fees are submitted: **BASIC NATIONAL FEE (37 CFR 1.492 (a)(1)-(5):** Neither international preliminary examination fee (37 CFR 1.482) Nor international search fee (37 CFR 1.445(a)(2) paid to USPTO And International Search Report not prepared by EPO or JPO..... $1,040.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by EPO or JPO.....$890.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International search fee (37 CFR 1.445(a)(2)) paid to USPTO..... $740.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) But all claims did not satisfy provisions of PCT Article 33(1)-(4).....$710.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) And all claims satisfied provisions of PCT Article 33(1)-(4)..... $100.00	**CALCULATIONS** PTO USE ONLY	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of **$130.00** for furnishing oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(e).	$130.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	16 -20=		X $18.00	$	
Independent Claims	2 -3=		X $84.00	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)				$	
TOTAL OF ABOVE CALCULATIONS =				$1020.00	
Reduction of ½ for filing by small entity, if applicable. A Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28).				$510.00	
SUBTOTAL =				$510.00	
Processing fee of **$130.00** for furnishing English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f).				$	
TOTAL NATIONAL FEE =				$510.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31).				$	
TOTAL FEES ENCLOSED =				$510.00	
				Amount to be refunded:	$
				charged:	$

a. ☐ A check in the amount of $ to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 04-0753 in the amount of $ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☐ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 04-0753. A duplicate copy of this sheet is enclosed.

d. ☒ A payment of $ 510.00 is made by credit card. A Credit Card Payment Form (PTO-2038) is attached hereto. The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 CFR 1.16 or any patent application processing fees under 37 CFR 1.17, or credit any over payment to the credit card account shown on the attached Credit Card Payment Form. Refund of all amounts overpaid, including those of twenty-five dollars or less, is specifically requested. Any fees not accepted by the credit card shown on Form PTO-2038 may be charged to Deposit Account No. 04-0753.

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SIGNATURE
Ira J. Schultz
NAME
28666
REGISTRATION NUMBER

Dkt. 01196

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Group Art Unit:

BINH VU THIEN et al Examiner:

Serial No.: National Phase of PCT/FR00/01297

Filed: concurrently herewith

For: METHOD AND DEVICE FOR EXTRACTION OF ELECTRODES IN A VACUUM AND EMISSION CATHODES FOR SAID DEVICE

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Before calculation of the filing fee, please amend the application as follows:

IN THE CLAIMS:

Please amend the claims as set forth hereinbelow and in the attached appendix:

1. (Amended) A method of extracting in a vacuum (4) electrons emitted from a cathode (2) situated in spaced-apart relationship with an anode (3) which is placed at a given potential relative to the cathode by means of a bias source (5), the method comprising:

· making a cathode (2) presenting at least one junction

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703 412-1155

(9) between a metal (7) serving as a reservoir of electrons and an n-type semiconductor (8), the cathode presenting an electron emission surface (11) possessing a surface potential barrier with a height of a few tenths of an electron volt (eV), and presenting thickness lying in the range 1 nm to 20 nm, defined by the value of the lowering desired for the surface potential barrier;

· injecting electrons through the metal/semiconductor junction (9) to create a space charge (Q) in the semiconductor (8) sufficient to lower the surface potential barrier of the semiconductor to a value that is less than or equal to 1 eV relative to the Fermi level of the metal (7); and

· using the bias source (5) that creates an electric field in the vacuum to control the height of the surface potential barrier (V_p) of the n-type semiconductor, so as to modify in reversible manner the electron affinity of the n-type semiconductor surface in order to control the emission of an electron flux towards the anode.

2. (Amended) A method according to claim 1, wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier (V_p) of the n-type semiconductor to be greater than the level of the states occupied by electrons in the n-type semiconductor so as to obtain an emission surface that does

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not emit electrons.

3. (Amended) A method according to claim 1, wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier (V_p) of the n-type semiconductor to be substantially equal to the level of the states occupied by electrons in the n-type semiconductor, in order to obtain an emission surface having low electron affinity.

4. (Amended) A method according to claim 1, wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier of the n-type semiconductor to be lower than the level of the states occupied by electrons in the n-type semiconductor so as to obtain an emission surface of negative electron affinity.

5. (Amended) A method according to claim 1 wherein the temperature of the cathode (2) is controlled in order to control the flux of the emitted electron beam.

8. (Amended) An electron emission cathode for a device for extracting an electron beam in a vacuum in accordance with claim 6, the cathode being characterized in that it comprises:

· a first portion forming an electron reservoir and constituted by at least one metal layer (7); and

· a second portion forming a conduction medium for the

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electrons injected into the metal layer and formed by an n-type semiconductor (8) co-operating with the metal layer to define a metal/semiconductor junction (9) possessing a potential barrier with a height of a few tenths of an electron volt, the n-type semiconductor presenting an emission surface (11) for the electrons, and possessing thickness lying in the range 1 nm to 20 nm defined by the value of the lowering desired for the surface potential barrier.

Please cancel claims 17 and 18 without prejudice or disclaimer of the subject matter thereof.

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REMARKS

The claims have been amended to delete all multiple dependencies and to otherwise place the claims in better form for US practice.

Respectfully submitted,

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APPENDIX

IN THE CLAIMS:

1. (Amended) A method of extracting in a vacuum (4) electrons emitted from a cathode (2) situated in spaced-apart relationship with an anode (3) which is placed at a given potential relative to the cathode by means of a bias source (5), the method [being characterized in that it consists in] comprising:

· making a cathode (2) presenting at least one junction (9) between a metal (7) serving as a reservoir of electrons and an n-type semiconductor (8), the cathode presenting an electron emission surface (11) possessing a surface potential barrier with a height of a few tenths of an electron volt (eV), and presenting thickness lying in the range 1 nm to 20 nm, defined by the value of the lowering desired for the surface potential barrier;

· injecting electrons through the metal/semiconductor junction (9) to create a space charge (Q) in the semiconductor (8) sufficient to lower the surface potential barrier of the semiconductor to a value that is less than or equal to 1 eV relative to the Fermi level of the metal (7); and

· using the bias source (5) that creates an electric field in the vacuum to control the height of the surface potential barrier (V_p) of the n-type semiconductor, so as to modify in

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reversible manner the electron affinity of the n-type semiconductor surface in order to control the emission of an electron flux towards the anode.

2. (Amended) A method according to claim 1, [characterized in that it consists in controlling] wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier (V_p) of the n-type semiconductor to be greater than the level of the states occupied by electrons in the n-type semiconductor so as to obtain an emission surface that does not emit electrons.

3. (Amended) A method according to claim 1, [characterized in that it consists in controlling] wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier (V_p) of the n-type semiconductor to be substantially equal to the level of the states occupied by electrons in the n-type semiconductor, in order to obtain an emission surface having low electron affinity.

4. (Amended) A method according to claim 1, [characterized in that it consists in controlling] wherein the bias source (5) is controlled so as to create an electric field suitable for causing the height of the surface potential barrier of the n-type semiconductor to be lower than the level

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